A DC-Coupled Neural Recording Analog Front-End with Bi-Level Bulk Modulation-Based EDO Compensation in 40nm Bulk CMOS

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***Abstract*—This paper presents a compact, low-power analog front-end (AFE) for high-density micro-electrocorticography (μECoG) recordings. The AFE integrates a DC-coupled, chopper-stabilized low-noise boxcar sampler, a passive switched-capacitor low-pass filter, and a 10-bit single-slope analog-to-digital converter (ADC). The boxcar sampler minimizes noise folding, enhances anti-aliasing and reduces chopping ripple. To prevent AFE saturation, a novel electrode DC offset (EDO) compensation loop is introduced. It features an embedded digital-to-analog converter (DAC) by modulating the bulk terminals of the input transistors, and a bi-level compensation scheme, thereby eliminating the requirements for high-resolution digital low-pass filters and explicit DACs typically used in traditional DC servo loops. Simulation results in 40nm bulk CMOS show an input-referred noise of 1.69 μV_{rms} over a 1–500 Hz bandwidth, an EDO compensation range of 110 mV_{pp}, with a power consumption of 2.28 μW and an estimated area of 0.0028 mm^2 per channel.**

***Index Terms*—Neural recording, analog front-end (AFE), micro-electrocorticography (μECoG), chopper stabilization, bi-level compensation (BLC), bulk modulation, electrode DC offset (EDO).**

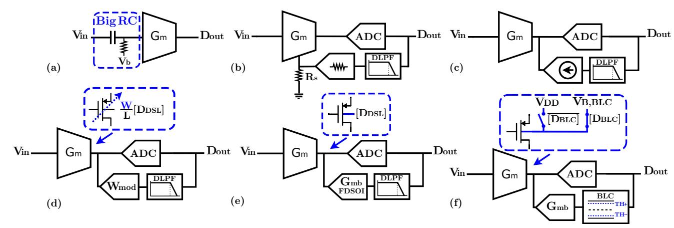
I. Introduction

Brain-computer interfaces (BCIs) have the potential to significantly advance therapies for neurological disorders and enhance our understanding of brain functions [1], [2]. Micro-electrocorticography (μECoG), where neural signals are recorded from the surface of the brain using sub-millimeter electrodes, is a promising technique to capture network-level information with neural circuit resolution. Future BCIs will greatly benefit from compact and low-power recording electronics that are capable of simultaneous recording from tens of thousands of electrodes.

Time-division multiplexing (TDM) directly at the recording electrodes allows for multiple electrodes to share a single analog front end (AFE), improving area efficiency while maintaining competitive power efficiency [3], [4]. However, TDM suffers from electrode noise folding due to the required higher AFE bandwidth, which can degrade signal quality. A dedicated AFE for each electrode improves scalability since it can maintain high signal integrity due to the close proximity of the sensing electrode and recording circuitry [5]–[7].

μECoG neural signals typically have an amplitude range from 10 μV to 1 mV and a band of interest from 1 to 500 Hz.

This work was conducted while Arnau Diez-Clos was at TU Delft; he is now pursuing a Ph.D. at CSEM.



	RC	RDAC	IDAC	Wmod	BDAC	Proposed
Area	X	X	X	✔	✔	✔
Noise	✔	X	X	X	✔	✔
STD CMOS	✔	✔	✔	✔	X	✔

Fig. 1: Mechanisms to filter or compensate the electrode DC offset: (a) AC Coupling, (b) RDAC, (c) IDAC, (d) Wmod, (e) BDAC, (f) proposed implementation.

However, a large unwanted electrode DC offset (EDO), resulting from electrochemical reactions at the electrode-tissue interface, can reach up to tens of mV. A key challenge in multi-channel neural signal acquisition is efficiently recording μV-level neural signals in the presence of large EDOs. Several techniques have been proposed to deal with the EDO without requiring an unnecessarily large dynamic range in the AFE.

AC-coupled amplifiers employ passive high-pass filtering at the AFE input for rail-to-rail EDO rejection [6], [8]–[10] (Fig. 1(a)). However, the high-pass pole needs to be set below 1 Hz to preserve low-frequency neural signals, which results in large passive components. Typically, the input capacitor becomes the dominant device in the AFE area. DC-coupled amplifiers with mixed-signal DC servo loops (DSLs) remove the need for input capacitors by moving the filter to the digital domain. The AFE output is low-pass filtered and subtracted from the input to create a high-pass filter. The subtraction can be implemented using either a resistor-based (Fig. 1(b)) [11], [12] or current-based (Fig. 1(c)) [13]–[15] digital-to-analog converter (DAC), which consumes area and introduces noise.

Another technique involves asymmetric tuning of the internal nodes in the input transconductance amplifier to generate an input-referred offset that counterbalances the EDO. In [16], this is accomplished by modifying the width of a transistor within the input pair (Fig. 1(d)). Although this method does not introduce additional thermal noise, flicker noise gets degraded in the presence of large EDOs. Reducing flicker noise requires the use of larger devices or a higher chopping frequency. In [4],

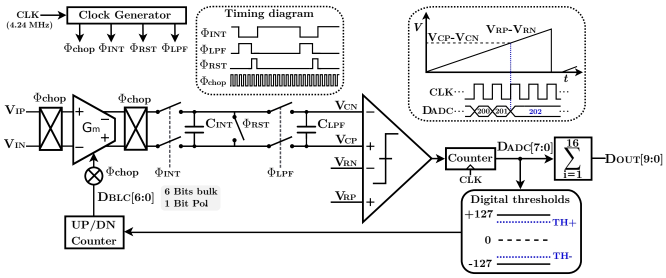


Fig. 2: Architecture of the proposed neural recording AFE.

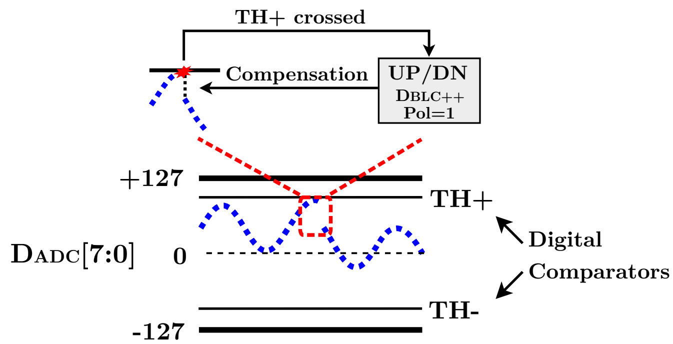


Fig. 3: Representation of bi-level compensation with a sinusoidal input signal and a gradually increasing EDO crossing the upper threshold.

the digital input is directly connected to the backgate terminals of a binary-split input transistor (Fig. 1(e)). This approach is very promising, but requires Fully Depleted Silicon on Insulator (FDSOI) technology to enable rail-to-rail driving of the backgate. Bulk-modulation EDO compensation in bulk CMOS technology has been investigated but current designs still rely on analog DSL, which is not area-efficient [17], [18].

This paper presents a highly scalable active digital pixel for neural recording AFE, featuring a novel bi-level bulk-modulation-based EDO compensation (Fig. 1(f)). The EDO compensation scheme is compatible with bulk CMOS technology and chopping modulation, and achieves 1.69 μV_{rms} input-referred noise in a [1-500] Hz bandwidth while consuming 2.48 μW per channel. Section II describes the system overview of the AFE design, Section III presents the simulation results, and the conclusions are drawn in Section IV.

II. Proposed AFE

A. Overview of the AFE design

The proposed AFE features a DC-coupled chopper-stabilized low-noise boxcar sampler (LNB) followed by a passive switched-capacitor low-pass filter (SC-LPF) and a single-slope (SS) analog-to-digital converter (ADC) - see Fig. 2. The LNB minimizes noise folding and improves anti-aliasing by introducing notches at multiples of the sampling frequency, which also attenuate the chopping ripple. Further high-frequency noise reduction is achieved by reusing the LNB integration capacitor (C_{INT}) as a switched-capacitor equivalent resistor to form a passive low-pass filter with the sampling capacitor (C_{LPF}). A continuous-time comparator compares the output of the SC-LPF with a globally distributed ramp to perform 8-bit quantization. The SS-ADC is oversampled (OSR=16) to achieve a Nyquist-rate (f_s = 1 kSps) resolution of 10 bits. The ramp generator can be shared across all pixels in an array, making its area and power consumption negligible when averaged across multiple channels, as demonstrated in [6]. A digital accumulator accumulates and decimates the digital output. All the timing signals required for the AFE are generated from a system clock (f_{clk} = 4.24 MHz) using a delay-based in-pixel clock generator. A novel EDO compensation loop is employed to prevent the saturation of the LNB due to the large EDO, and its functionality is described in the following section.

B. Amplifier with embedded EDO compensation

1) Control loop: The proposed approach avoids the need for the high-resolution digital low-pass filter used in mixed-signal DSL architectures to extract the EDO. Instead, it compares the 8-bit oversampled digital output of the ADC (D_{ADC}) with upper and lower programmable thresholds (TH_{+} and TH_{-} respectively) to control the EDO compensation loop [4], [19]. If the AFE input range is larger than the expected neural signal, a digital output close to either extreme indicates a large EDO at the input. In practice, if the output crosses the upper (lower) threshold, a 6-bit digital accumulator (D_{BLC}) is incremented (decremented) by 1 LSB (Fig. 3). D_{BLC} directly controls the compensation DAC to compensate the EDO until the net input falls within the AFE's linear input range. The control loop also keeps track of the polarity of the EDO.

A change in the compensation DAC introduces a DC jump (discontinuity) in the output signal. However, due to the gradual slow EDO drift, these discontinuities occur very infrequently and can easily be corrected in signal post-processing, resulting in a minimal impact on the acquired signal [20].

2) EDO compensation embedded DAC: The bulk terminals of the PMOS input devices in the OTA are modulated to induce an offset that compensates the EDO. The input transistors are split into N = 6 binary weighted parallel devices with independent N-wells. Depending on D_{BLC}, each bulk terminal is either connected to the voltage supply (V_{DD}) or a low-impedance node $V_{B,BCL} < V_{DD}$ (Fig. 4).

The bulk terminals of the input transistors are controlled according to the polarity bit to compensate for both positive and negative EDOs. When there is a positive EDO, the positive input transistors are controlled by D_{BLC}, while the bulk of the negative input transistors are connected to V_{DD}. The opposite happens for a negative EDO.

The generated input-referred offset (IRO) to compensate the

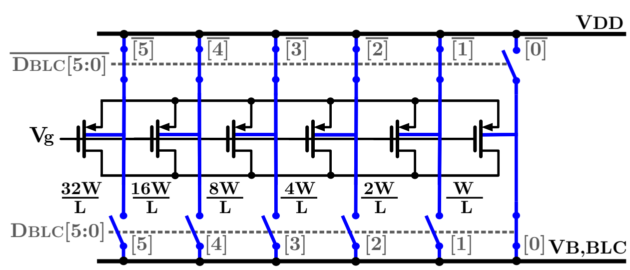


Fig. 4: Proposed bulk modulation for the input transistors with example code D_{BLC} = "000001".

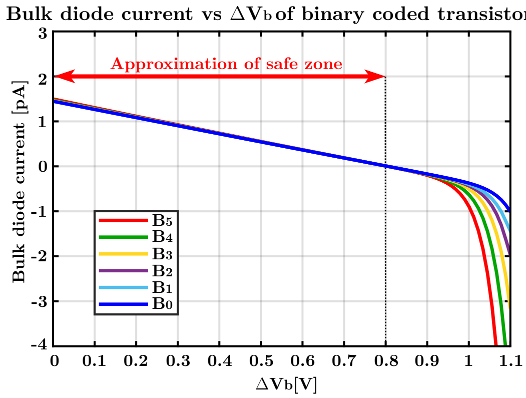


Fig. 5: Bulk diode current as a function of Δ_{V_b} for all binary coded PMOS devices.

EDO is derived as

$$IRO = \frac{g_{mb}}{g_m} \cdot \frac{\Delta V_b \cdot \sum_{i=0}^{N_{BLC}-1} D_{BLC}[i] \cdot 2^i}{2^{N_{BLC}}} \tag{1}$$

where g_{mb} is the backgate transconductance of the input transistor, $\Delta_{V_b} = V_{DD} - V_{B,BLC}$ and N_{BLC} is the number of DAC bits.

Equation (1) represents a linear relationship between the input-referred offset and the control variables. However, the system's behavior is not entirely linear since the input transistors are biased in the subthreshold region to improve power efficiency. This does not pose a problem as long as the response remains monotonic. However, the largest step between codes (i.e., largest residual EDO) must be carefully considered when designing the redundancy in the AFE input range to ensure a reliable operation.

A higher Δ_{V_b} allows for a higher EDO compensation range. At the same time, a lower Δ_{V_b} reduces the residual EDO after compensation. Also, Δ_{V_b} needs to be carefully controlled to avoid forward biasing the bulk to drain/source junctions. Similarly, splitting the input transistor into a higher number of devices can increase the compensation resolution, but increases the overall area of the OTA. In this design, the input transistors are split into 6 binary-weighted devices and Δ_{V_b} = 230 mV, which is in the safe zone of operation (Fig. 5). This leads to an EDO compensation range of $\pm$55 mV, with a maximum residual EDO smaller than 1.5 mV (Fig. 6).

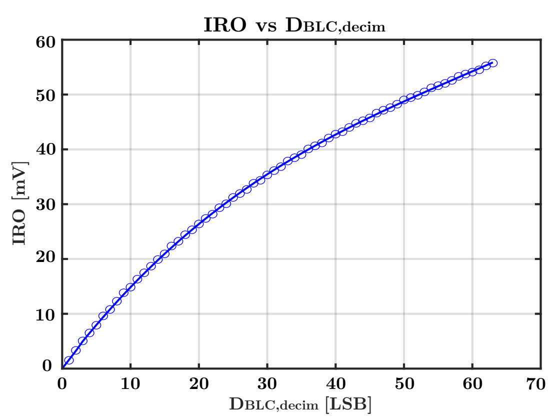


Fig. 6: IRO vs BLC code with a 6-bit embedded DAC and Δ_{V_b}=230 mV.

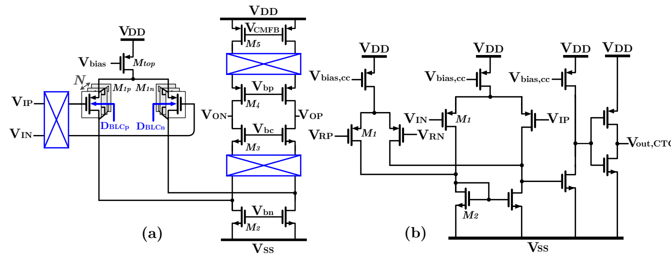


Fig. 7: (a) Circuit schematic of the implemented chopper stabilized OTA with binary-coded input transistors (the SC-CMFB is not included in the figure), (b) Circuit schematic of the CT Comparator with four differential inputs to single-ended output.

Notably, the chopper input switches up-modulate the input signal, which also up-modulates the EDO (see Fig. 2). Therefore, the compensation DAC must also be chopped. This is achieved through a switching scheme where the bulk connections of the positive and negative input transistors are alternated with the same frequency as their gates, ensuring that the bulk feedback is chopped synchronously with the input signal.

C. OTA and CT comparator

The OTA uses a fully differential folded cascode topology (Fig. 7(a)) to achieve large output impedance (>300 MΩ from simulations). The input transistors are thick oxide devices to reduce gate leakage and are biased in weak inversion (I_D = 400 nA) to obtain a transconductance g_m = 10 μS to meet the thermal noise requirements. A switched-capacitor-based common mode feedback (SC-CMFB) is used to stabilize the output common-mode voltage to $V_{cm} = \frac{V_{DD}}{2}$.

The OTA employs chopper stabilization to suppress flicker noise effectively. The up-modulation takes place at the input, while the de-modulation is placed at the internal cascode nodes of the output branch (Fig. 7(a)), to avoid reducing the output impedance. The chopping frequency is set to $f_{\text{chop}} = 50\,\text{kHz}$ to coincide with one of the notches introduced by the LNB (see Fig. 8) and to balance flicker noise reduction and input impedance degradation.

The continuous time comparator (CTC) used for the SS-ADC is implemented with two fully-differential inputs for the outputs of the LNB and the ramp signal and a single-ended output (shown in Fig. 7(b)). Typically, an auto-zero mechanism is needed to cancel the input-referred offset of the comparator [6]. However, in the proposed design, the input-referred offset from the comparator is automatically compensated by the EDO compensation loop.

III. Simulation Results

This work was simulated (pre-layout) in 40nm bulk CMOS technology. The AFE achieves a mid-band gain of 43.6 dB (Fig. 8). Fig. 9(a) shows the simulated output spectrum of the AFE when a 100 Hz, 1 mV$_{\text{pp}}$ sine wave is applied at the input. Under these conditions, the AFE achieves a peak SNDR and SFDR of 43.3 and 52.5 dB. The input-referred noise (IRN) improves from 14.48 μV$_{\text{rms}}$ to 1.69 μV$_{\text{rms}}$ over 0.5-500 Hz when chopper stabilization is activated (Fig. 9(b)). The AFE power consumption is 2.48 μW (Fig. 10(a)), with

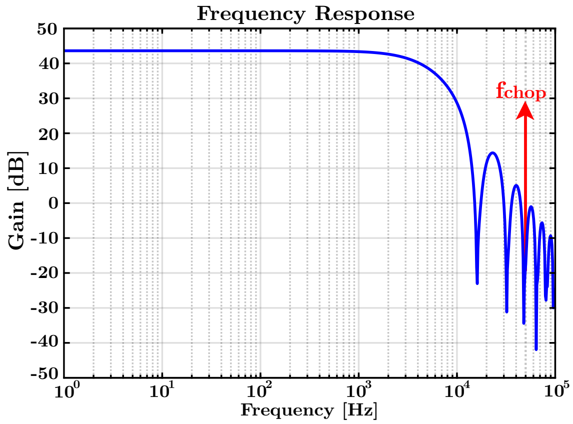


Fig. 8: Frequency response of the LNB and SC-LPF with a mid-band gain of 43.6 dB. The chopping frequency (f_{chop}) is set to 50 kHz to coincide with one of the notches introduced by the LNB.

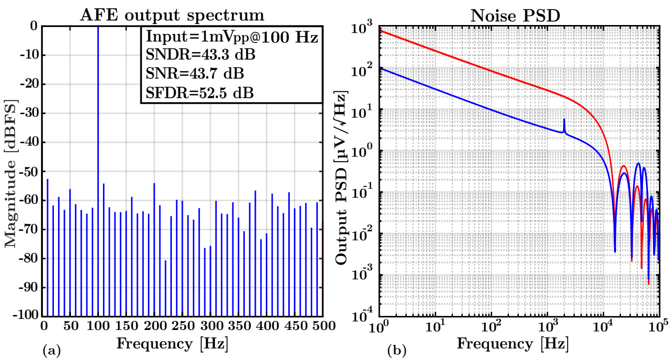


Fig. 9: (a) AFE Output spectrum with a 100 Hz, 1 mV_{pp} input sine wave obtained from a 100 ms transient (10–110 ms) using a rectangular window, with a frequency range of 10–500 Hz, (b) Output noise power spectral density (PSD) of the LNB and SC-LPF with chopping OFF (red) and with chopping ON (blue).

an estimated area from preliminary layout of 0.0028 mm^2 (Fig.10(b)). The EDO compensation range is 110 mV_{pp}, with a total harmonic distortion (THD) of -52.74 dB for 1 mV_{pp} signals. It achieves a common-mode rejection ratio (CMRR) of > 80 dB in-band while the input impedance (Z_{in}) is > 70 MΩ. Fig. 11 demonstrates the compensation loop functionality with an input sine wave on top of a rapidly increasing EDO (accelerated for the simulation) crossing TH_+, triggering an increment in D_{BLC} and bringing the input signal back to its linear region.

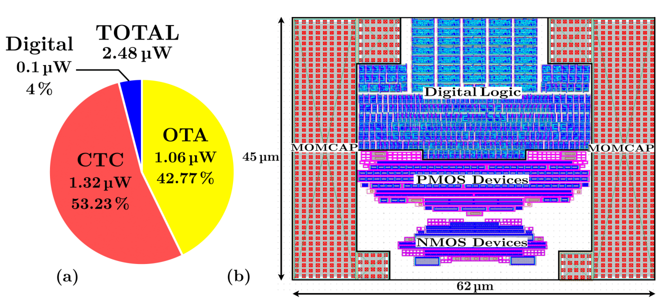


Fig. 10: (a) AFE power breakdown, (b) Estimated area from a preliminary layout with adjacent AFE components, excluding routing, spacing, and other factors that may increase the final area. Shared components such as the global ramp generator and biasing circuitry, distributed across multiple AFEs, are not considered.

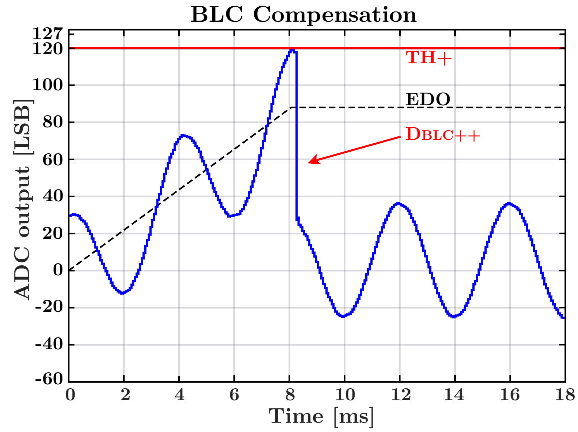


Fig. 11: BLC Compensation with a 250 Hz, 1 mV_{pp} sine wave on top of an increasing EDO (in blue). The EDO (in black) increases from 0 mV to 1.5 mV over 8 ms. TH_+ (in red), is set +120 LSB.

TABLE I
COMPARISON WITH OTHER (μ)ECOG READOUT CIRCUITS.

Reference	JSSC'15 [21]	SSCL'18 [15]	JSSC'22 [3]	JSSC'22 [4]	TBioCaS'24 [7]	THIS WORK
Topology	AC-LNA + VCO ADC	DC-VCO ADC	AC-LNB + SAR ADC	AC-I-ΔΣ	DC-I-ΔΣ	DC-LNB + SS ADC
Technology [nm]	65	65	65	22	180	40
Supply [V]	0.5	0.6	1.2	0.8	1.8	1.1
Multiplexing	NO	NO	256:4	256:16	NO	NO
Channel Count	64	1	256	256	1	1
Bandwidth [Hz]	500	500	500	500	7500	500
IRN [μV_{rms}]	1.2	2.2	3.2	1.55	1.46[a]	1.69
Area/Ch. [mm^2]	0.025	0.01	0.004	0.001	0.03	0.0028[b]
Power/Ch. [μW]	2.3	3.2	1.51	1.61	24.7	2.48[c]
Input [mV_{pp}]	6	-	2.5	5	20	4
THD [dB]	-48 (1 mV_{pp})	-	-	-53 (2 mV_{pp})	-70.3 (20 mV_{pp})	-52.74 (1 mV_{pp})
CMRR [dB]	88	77	70	98	-	80.94
Z_{in} [MΩ]	28 (100 Hz)	>500	24.5 (100 Hz)	43[d]	216	71.4 (100 Hz)
EDO Tol. [mV_{pp}]	98.6	93	100	156.6	200	110

[a] Measured from 1-200 Hz
[b] Estimated based on AFE preliminary layout
[c] Shared components across the AFE array not included
[d] Estimated at electrode (i.e. measured at ASIC and referred to the multiplexer input)

IV. CONCLUSION

This paper presents a novel AFE for high-density μECoG neural recordings. The key innovation is a Bi-level compensation (BLC) loop that compensates EDOs by directly modulating the bulk of the OTA's input transistors. This approach eliminates the need for bulky AC coupling capacitors, and high-resolution digital low-pass filters and additional DACs required for mixed-signal DSLs, resulting in a compact, low-power design suitable for high-density recording arrays. The proposed design, which integrates a DC-coupled chopper-stabilized low-noise boxcar sampler, a passive switched-capacitor low-pass filter, and a single-slope ADC with a globally distributed ramp, achieves competitive performance in terms of noise, power, CMRR, and THD (see Table I), even when compared to designs leveraging multiplexing techniques. Notably, the estimated area per channel is significantly smaller than other single-channel designs, up to 3× to 10× more compact, while maintaining a wide EDO compensation range and high input impedance.

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