

A 22 nm, 6-9 GHz ADPLL for UWB Ranging and Communication Applications

V. Kopta, F. Chicco

The demand for Ultra-WideBand (UWB) radio is growing since its inclusion in smartphones and is expected to continue along this path in the future, driven by the demand for precise and secure localization in various applications. One of the most challenging parts of any UWB radio is the frequency synthesizer that covers the needed frequency range in the high UWB band, while minimizing power consumption.

UWB is a proven technology that enables high-precision ranging and localization, in harsh multipath propagation conditions, making it an ideal candidate for indoor asset tracking and real-time localization systems. The centimeter-level precision is achieved using extremely short pulses that minimize interference and maximize temporal resolution. With the growing demand for accurate localization in sectors like smart homes, warehousing, automotive and healthcare, the demand for UWB is expected to grow in the coming years. CSEM has a long experience with the UWB technology through internal development and collaboration with external partners. One of the key parts of a UWB radio is a frequency synthesizer, implemented as a phase locked loop (PLL), that generates the precise internal clocks or the high-frequency carrier signal used for transmission in the Tx mode or downconversion of the received signal in the Rx mode.

The implemented PLL is an all-digital PLL (ADPLL) that uses digital control loop and a time-to-digital (TDC) converter to detect the output frequency and provide phase locking. Compared to the standard analog PLL, the ADPLL is more easily portable to different technology nodes. The digital loop filter typically occupies a significantly smaller area and is configurable, providing the freedom to optimize the phase noise (PN) and dynamic performance in different modes of operation. The TDC is assisted by a digital-to-time converter (DTC) allowing to reduce the range and power consumption of the TDC that operates at the divided Digitally-Controlled Oscillator (DCO) frequency [1]. To cover a broad frequency range the TDC is preceded by a configurable frequency divider that assures that the input frequency falls into the range of the TDC. Each analog block of the PLL is supplied by a separate LDO to isolate different analog blocks from the external supply and minimize coupling between the internal supplies.

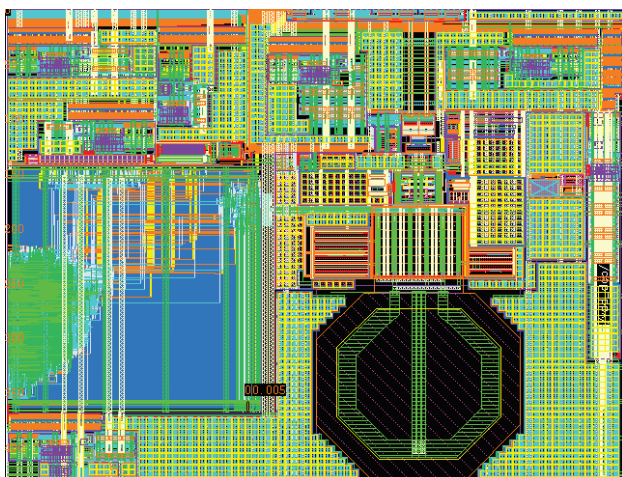


Figure 1: ADPLL layout.

The ADPLL layout is shown in Figure 1, it occupies an area of 0.24 mm² and is implemented in the 22 nm technology node. A significant area is used for the LDOs, as well as the needed decoupling capacitors and the digital controller.

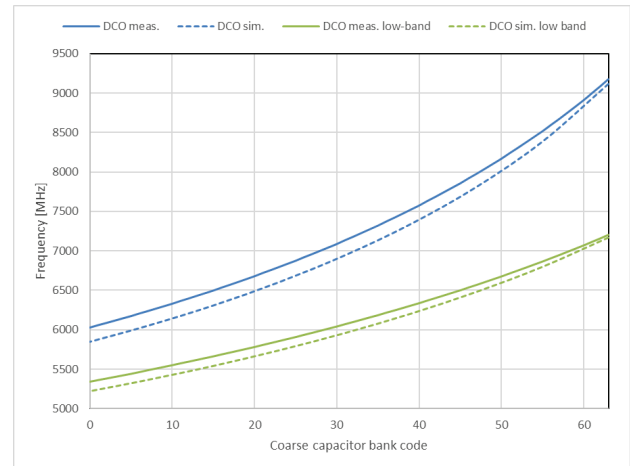


Figure 2: DCO frequency range in the two modes of operation.

The DCO operates at twice the carrier frequency. This is done to reduce coupling to the power amplifier and reduce pulling, and to allow for quadrature signal generation. The DCO is a complementary cross-coupled LC oscillator, that requires a lower current compared to more common NMOS or PMOS-only oscillators. Amplitude feedback is used to guarantee a constant output amplitude over a large frequency range. The DCO frequency range is shown in Figure 2. In the normal mode of operation, the DCO covers the frequencies in the upper UWB band, from 6 GHz to 9 GHz. This range is sufficient to cover the two mandatory channels, channel 5 at 6.489 GHz and channel 9 at 7.987 GHz. The "low-band" option can be used for the narrow-band (NB) radio intended to assist the UWB (NBA-UWB), by extending the link budget and offloading the clock offset estimation and communication to a lower power radio. It operates in the two bands centered at 5.8 GHz and 6.2 GHz, as defined by the UWB standard. In the future these bands are likely to be shared with the Bluetooth extension to 6 GHz, hence expanding the range of possible applications of the PLL. The ADPLL consumes between 10 mA and 14 mA over the wide frequency range of interest. A large portion of the power budget is consumed by the high-speed dividers and buffers that drive the power amplifier and the mixers.

[1] V. K. Chillara, et al., An 860 μ W 2.1-to-2.7GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth Smart and ZigBee) applications, ISSCC (2014)