COSETE – Cooperative Sensors for Electrical Impedance Tomography

A. Fivaz, B. Sporrer, O. Chételat, D. Besse

CSEM's cooperative sensors (CS) are designed to equip medical devices for long-term patient monitoring and everyday use. They are miniature sensors capable of electrographic imaging and electrical impedance tomography (EIT). Arranged in a two-wire parallel bus configuration, they achieve an outstanding level of integration in wearables requiring multiple electrodes. The present article reports the ongoing implementation of the bioimpedance electronics front-end which, in conjunction with biopotential measurement developed in previous activities, should enable regional cardiopulmonary function using EIT such as the pulmonary artery pressure (PAP), a method patented by CSEM. In the future the device will be extended to provide electrical impedance spectroscopy (EIS), a feature that is required for non-invasive continuous glucose monitoring (NiCGM) which is an upcoming methodology already patented by CSEM.

Monitoring PAP or NiCGM requires EIT imaging with multiple sensors, and the belt prototype shown in Figure 1, currently under development, provides for this purpose 25 sensors placed around the thorax.

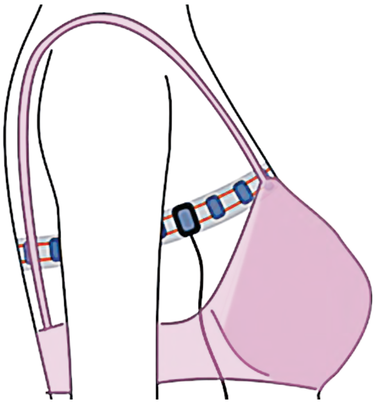

Figure 1: EIT belt prototype in development.

The sensors are composed of an application-specific integrated circuit (ASIC) with just a few surrounding components and a housing. They will look like the cooperative sensor for biopotential measurement developed previously and shown in Figure 2. The ASIC is packaged in a prototyping case and currently requires a size of 7×7 mm^2. Further size optimizations are possible.

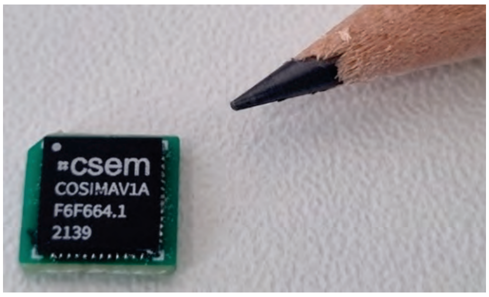

Figure 2: Sensor board prototype for biopotentials (similar formfactor for EIT sensor in development).

The measurement of impedance is achieved by multiple sensors working in tandem. Two sensors inject alternating currents i with equal amplitude, but opposite phase, into the body. The resulting voltages are then measured by all other sensors providing enough information to compute an EIT image, i.e., an impedance map of a cross-section of the thorax. The technical challenge is to resolve the resistance on the injection path within $\rho = 5$ mΩ (rms) in a 2 Hz bandwidth. From the following equation, where N is the number of stimulation patterns and v the electronic noise of the acquisition chain:

$$\rho = 2\sqrt{N}\frac{v}{i}$$

the only ways to reduce ρ without relying only on the reduction of the noise v of the acquisition chain are to limit the number of patterns N, which in turn reduces the resolution of the imaging, and to use the highest possible injection current i, which is however limited by the voltage range provided by the current source i and the dry electrode/skin impedance. With a value of $i = 100$ µA (rms), a target specification of $\rho = 5$ mΩ (rms) and $N = 25$ patterns, as a typical example, this requires a noise floor for the acquisition chain of only $v = 50\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$ (comparable to the noise floor of a single 100 kΩ resistor). This is a challenging noise specification for ultra-low power microelectronics. Moreover, the stringent noise limit also applies to any distortion and perturbation picked up by the circuit, e.g., through coupling from other blocks within the ASIC.

Since each sensor has a single electrode, the electrode potential acquisition is obtained against a reference voltage. In a 2-wire CS system the only available reference is the system ground wire (see Figure 3), which also serves as the return path for all powering and signals currents, for all sensors in the system. Over the finite impedance of the bus this leads to the occurrence of interference signals. In this work, the design is optimized to maximize the rejection of out-of-band perturbations by providing strong filtering before any chopping or sampling operation is conducted. In scenarios where this is not expected to lead to sufficient suppression (e.g., when powering frequency and EIT signal frequency are too close to each other) an alternative approach is obtained with the same ASIC but with one additional wire (in blue in Figure 3) so the current return and potential reference functions are implemented by two separate wires. This mitigation measure avoids the possibility of wire crosstalk in the system.

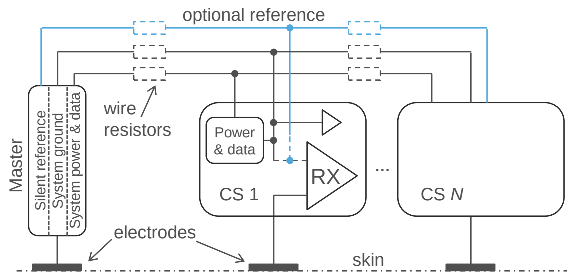

Figure 3: CS implementation showing the optional use of a third wire (in blue) to mitigate the risk of crosstalk.

A test chip will be produced in early 2025 and belt prototypes will be manufactured and tested later in the year.