A Miniature Timing Microsystem Using two Silicon Resonators

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A miniature timing microsystem based on a pair of co-integrated low and high frequency silicon resonators is reported. It can be used to generate a μW-level accurate, low power, real time clock (RTC) and low jitter clocks at any frequency between 1-50 MHz at less than 10 mW power dissipation.

In recent years, the timing industry, which has been dominated by quartz for several decades, has been continuously challenged by the introduction of new products based on MEMS resonators. Such timing solutions offer interesting miniaturization perspectives with eased packaging accomplished at wafer or chip-scale level using silicon manufacturing lines. This paper address such challenges with the demonstration of co-integrated AlN-actuated silicon resonators combined to an ASIC to derive both a low power, low frequency clock to generate a real time clock (RTC) and low noise, low jitter programmable clocks between 1-50 MHz.

Figure 1 shows a detailed block diagram of the timing microsystem [1]. A low frequency 430 kHz silicon resonator based oscillator combined intermittently to a temperature sensitive 10 MHz RC oscillator is used to derive a temperature-compensated 32,768 Hz clock after fractional division (÷R) for frequency adjustment (~1ppm over 2s). The 32,768Hz signal drives the real time clock (RTC) sub-circuit implementing clock, calendar, timer and alarm functions. Besides the RTC, HF clocks re-programmable between 1 to 50 MHz via a serial interface can be generated on demand using a 26 MHz silicon resonator-based oscillator combined to a fully integrated fractional PLL (divider N, Phase Frequency Detector, Charge Pump and Loop Filter). Up to two independent temperature compensated clocks with low noise and low jitter performance, such as required for radio applications or high dynamic range converters are obtained after integer (÷M) or fractional division (÷P) of the LO signal that is compensated by adjusting the N division ratio in a temperature dependent way. Two output pads are available to multiplex the HF clocks.

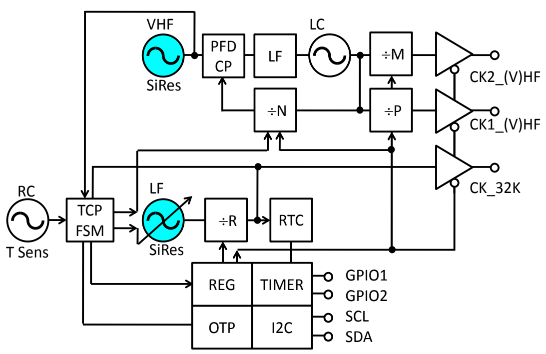

Figure 1: Architecture of the timing microsystem.

Figure 2 shows photographs of the microsystem components at similar scales together with an illustrative cross-section of the packaging concept which is still under development. Post-processed CMOS wafers featuring through via connections (TSV) are used as part of the package to reach extreme miniaturization. The silicon resonators are then assembled on the backside of the CMOS wafer after deposition of the appropriate sealing and contacting layers yielding a 300 μm-thick module that could be flip-chip bonded on a PCB.

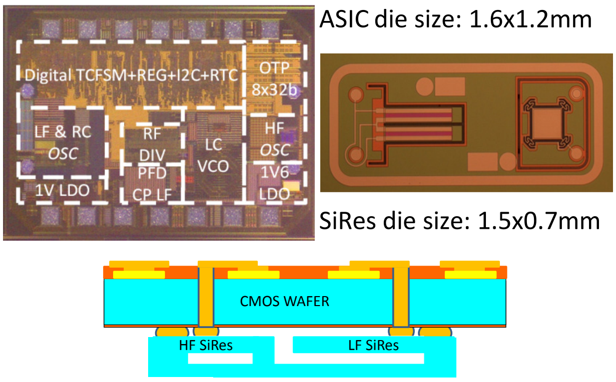

Figure 2: Microsystem components and illustrative cross-section.

Figure 3 shows a phase noise measurement of the HF clock generation circuit achieved as part of an early system level validation. The 26.36 MHz SiRes-based clock is plotted together with the LC VCO divided clock exhibiting the characteristic $\Delta\Sigma$ modulator induced quantization noise shaping. The LC PLL is locked via the fractional-N divider at 2.16 GHz from which a low noise 48 MHz clock is obtained by integer division by M=45. Apart in the vicinity of the loop filter bandwidth (200-300 kHz), the generated clock phase noise tracks the reference noise with a scaling of 20 log(N/M) as expected. The current consumption is 5.6 mA at 1.6 V (9 mW) shared evenly between the 2.16 GHz LO, the two N and M dividers including the PFD/CP, $\Delta\Sigma$ modulator and 26 MHz MO reference and the on-chip buffer driving an on-board 50Ω driver.

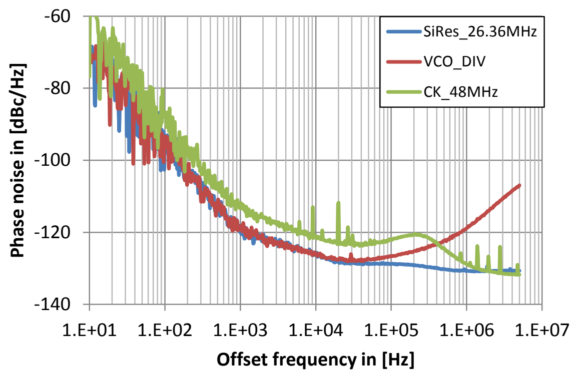

Figure 3: HF clocks phase noise measurement.

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[1] D. Ruffieux, *et al.*, "A miniature timing microsystem using two silicon resonators, " in Proc. of the IEEE Frequency Control Symposium, (2013) 1