A Low-jitter Reference-less Clock and Data Recovery (CDR) with Low Phase-noise Multi-clock Generation

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This paper reports the development of an integrated 2.7 GHz reference-less Clock and Data Recovery (CDR) circuit with an ultra-low phase-noise multi-clock generator for low-jitter and high-speed clocking applications.

Our recent development towards a low-noise Phase-Locked Loop (PLL) [1] demonstrated 20 dB in-band and 9 dB out-of-band phase noise improvement at a moderate increase of power dissipation compared to CSEM's legacy ULP short range RF-synthesizer expertise. This follow-up work aims at substituting the crystal reference clock with the recovered clock of a Clock and Data Recovery (CDR). This enables cascading multiple devices in a chained configuration, collecting data from individual nodes at the ring's end, while avoiding the need to manage individual crystals and their frequency imprecision. This simplifies network synchronization and reduces costs. Besides guaranteeing wireline communication at 900 Mbps, the focus was obtaining low-noise clocks for medical applications.

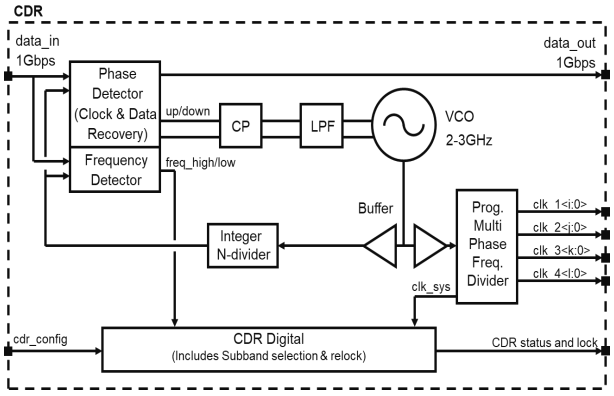

Figure 1: Block diagram of the proposed CDR with ultra-low phase noise multi-clock generation.

This report presents the design of a 900 Mbps low-power reference-less CDR with an ultra-low phase-noise programmable multi-clock generator. The simplified block diagram is illustrated in Figure 1. Contrary to conventional PLL-based CDR's, the proposed architecture does not rely on a crystal oscillator (XO) but rather extracts the timing reference of the system directly from the input data. The loop is composed of a linear Triwave Hogge Phase Detector (PD), a Charge Pump (CP), a 1nF integrated loop Low Pass Filter (LPF), a 2.1 to 3.2 GHz Voltage-Controlled Oscillator (VCO), an integer loop frequency divider and a Frequency Detector (FD). To address a large domain of applications requiring high-performance clocks, the CDR is complemented with versatile ultra-low phase-noise frequency dividers all synchronized by the data recovered clock. It features various division ratios, each with multi-phase clock generation for phase sensitive applications. It also generates the system clock. Automatic sub-band selection during first lock, continuous lock status tracking, and automatic re-lock in case of unlock detection is performed thanks to a novel digital finite state machine assisted rotational phase FD, capable of operating over a wide frequency range to overcome variable data rates and data-dependent run-lengths. The complete CDR including the programmable frequency divider, at the exception of the bandgap current reference is supplied from a 1.1 V source.

One of the key performance parameters to optimize in CDR's is the data jitter transfer function to guarantee minimal amplification of the jitter, particularly, in applications where multiple chips and thus CDR's are cascaded one after the other. Hence, the proposed CDR is designed for jitter peaking minimization, while providing an excellent phase noise performance both in-band and out-of-band.

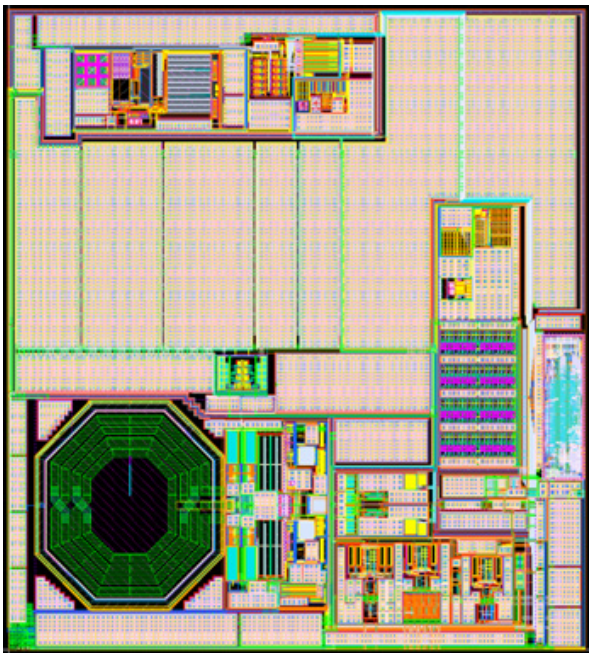

Figure 2: Layout view of the CDR IP.

Figure 2 shows the layout view of the CDR. The circuit, with a footprint of 800×885 µm, was integrated in a low-power RF 40 nm technology. The CDR and the programmable frequency divider consume 20 mA from a 1.1 V supply. Simulation results predict an intrinsic clock-driven RMS absolute jitter of 300 fs with an integrated bandwidth from 1 kHz to 100 MHz at 2.7 GHz. The long-term N-period jitter at 1 ms is 750 fs and the closed loop jitter peaking is <0.5 dB.

[1] C. Salazar, *et al.*, "A frequency synthesizer for ultra-low phase noise multi-clock generation", CSEM Scientific and Technical Report (2019) 111.