A Dual-mode Bluetooth Transceiver with Two Concurrent RX Paths, Offset-LO, +20 dBm Output Power, and -98 dBm Sensitivity in GF22 FDSOI

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A Dual-mode Bluetooth transceiver with two concurrent receive (RX) paths for the simultaneous reception of BT and ZigBee is presented. It achieves +20 dBm maximum output transmit power and -98 dBm Sensitivity in BLE 1 Mbps. An offset local oscillator (offset-LO) alleviates pulling.

Compared to the icyTRX-DM, which has a single RX path and delivers +10 dBm maximum output power, this IP offers two RX chains to receive BT (BLE, BR, EDR2, EDR3) and Zigbee simultaneously. The tenfold increase in the output power necessitated 1) the redesign of the digital power amplifier (DPA) to keep the same supply voltage, 2) the rework of the antenna interface to protect the receiver's front end during transmission, and 3) the introduction of an offset-LO scheme to alleviate pulling. Furthermore, the requirement for concurrent reception drove the choice of current-mode RX paths due to their superior linearity. The IP was implemented in the GF22 FDSOI process and occupies two square mm. The block diagram is shown in Figure 1. The layout is depicted in Figure 2.

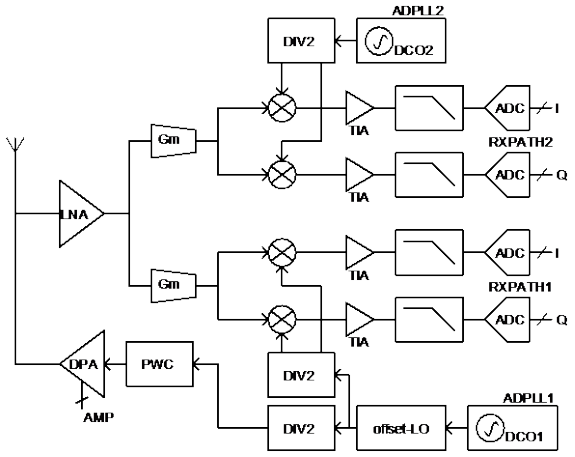

Figure 1: Block diagram.

The first all-digital phase-locked loop (ADPLL1) and the Offset-LO operate when the transmitter is on and ensure that the digitally controlled oscillator DCO1 does not run at an integer multiple of the DPA frequency, thus eliminating pulling. The DCO1 operates in the 3.2-3.3 GHz range and drives the offset-LO, which outputs 4.8-4.96 GHz. The offset-LO consists of an active single-sideband mixer with an inductive load to keep the levels of the generated spurs well below the DPA harmonics. A divide-by-2 (DIV2) generates the required 2.4-2.48 GHz LO signal for the DPA. The phase noise of the offset-LO is designed to be well below the phase noise of the DCO1. The ADPLL1 is also used during the receive operation to generate the LO signals for the first RX path (RXPATH1), while the ADPLL2 generates the LO signals for the second RX path (RXPATH2). The DCO2 operates at twice the LO frequency. The phase noise of the DCOs is -110 dBc/Hz at 1 MHz offset, and each ADPLL dissipates about 1.5 mA. Both DCOs use Fig-8 inductors to minimize magnetic coupling.

A digital inverse class-D power amplifier with an integrated balun provides up to +20 dBm at the antenna. Phase modulation generated within the ADPLL1 feeds directly to the DPA's phase path, which consists of a divide-by-2 (DIV2) and a pulse-width control block (PWC) that offers an additional knob to set the output power and minimize the level of the DPA second harmonic, easing the design of the external harmonic filter. Amplitude modulation for EDR2 and EDR3 is introduced by dynamically controlling the DPA's 256 slices. Being an RF DAC, it generates aliases in the output spectrum. The amplitude data (AMP) are fed into the DPA at a high rate (400 MHz) to alleviate this effect and meet the out-of-band emission requirements. For constant envelope modulations (BLE, BR, ZigBee), the number of active slices is statically set to control the output power level. AM-AM and AM-PM predistortions are implemented in the digital portion of the IP. Typical maximum output power is +20 dBm with 30 % system efficiency from a 1.8 V external supply.

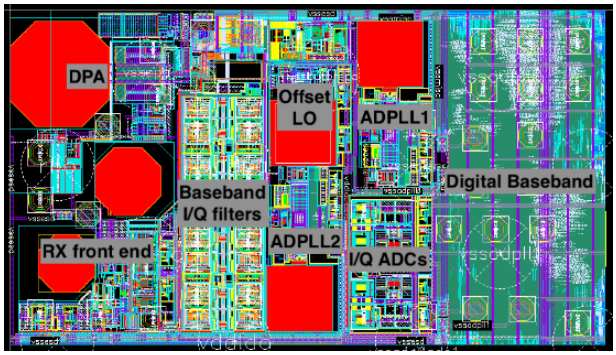

Figure 2: Layout view. The total area is two square mm.

The two low-IF receive paths consist of a common front end connected at the negative side of the DPA balun, shorted to the ground by the integrated TX/RX switch during transmission to protect it from the high swing at the antenna. ESD diodes protect the RX/TX switch. The front end is based on an inductively matched common-gate LNA with an additional inductor in the load tank for good noise performance. The LNA drives two current-mode 25% I/Q passive mixers via transconductance stages (Gm), followed by transimpedance amplifiers (TIA). The TIA outputs feed directly into the baseband analog filters. DC offset calibration is achieved by adjusting the back-gates of the differential pairs at each filter input. The filter cutoff frequency is set to 2 MHz or 4 MHz, depending on the modulation format. Digitization is done with two (per-path) 9-bit SAR ADCs sampled at 48 MHz. Peak detectors along the two RX chains facilitate automatic gain control. The overall gain of each receive path is 72 dB while achieving 5.5 dB NF to meet the -98 dBm sensitivity specification for BLE 1 Mbps. Power dissipation is 2.9 mA for both paths simultaneously and 2.1 mA for single-path operation.

The IP's RF architecture has been reused in the latest versions of the icyTRX-DM in both GF22 FDSOI and TSMC22 bulk processes, albeit at a reduced output power level and with a single RX path and no offset-LO.