Sensor Interface ASIC for Heart Rate and SPO2 Measurement

P. Persechini, F. Giroud, R. Gentsch, T.-C. Le, C. Monneron, N. Raemy, P.-F. Ruedi, P. Theurillat

Starting from an existing prototype developed at CSEM with off-the-shelf electronic components, the Pulsemon project has for objective to deliver an ASIC that embeds on a single silicon die a heart rate and SPO2 measurement platform. Enabling deeper miniaturization and power consumption reduction, the ASIC uses the same architecture based on the photoplethysmography and the absorption spectroscopy of the blood.

CSEM has previously developed a system based on discrete electronic components (Pulsewatch [1]) wearable on the wrist (in a watch) allowing measurement of the Heart Rate (HR) and the Pulse Oxygen Saturation (SPO2).

The HR extraction uses the PhotoPlethysmoGraphy (PPG). An InfraRed (IR) Light-Emitting Diode (LED) lights up the skin while a photodiode detects the variations of the emitted light. As this light is disturbed by blood volume changes, electrical variations in the photodiode are related to the heartbeat.

The SPO2 extraction uses the absorption spectroscopy of the blood. An IR LED and a Red LED are used alternatively while a photodiode analyses the incoming light. When blood is saturated with oxygen, IR light is absorbed whereas Red light is reflected and reversely. The ratio between the reflected amount of light coming from the Red LED and the IR LED into the photodiode is proportional to the blood oxygen saturation.

The objective of the present development is to integrate into an Application Specific Integrated Circuit (ASIC) the existing system. The ASIC should implement all the functions of the analog chain that is Trans-Impedance Amplification (TIA), Ambient Light Removal (ALR), Low-Pass Filtering (LPF), Sample-and-Hold (S&H) and Voltage Gain Amplification (VGA). LED drivers and Analog-to-Digital Converter (ADC) are also included as well as a sequencer for synchronization and an SPI interface. The ASIC allows a high level of miniaturization with few external components and is optimized in term of power consumption.

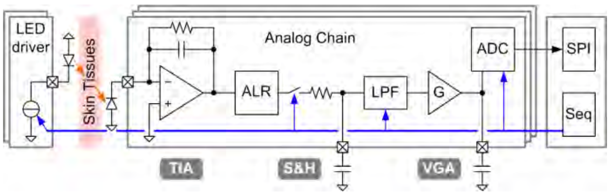

Figure 1: Schematic principle of one analog chain and LED driver.

The analog chain described in Figure 1 is copied three times. Two chains are needed to measure separately the Red and IR light from the related LEDs in the SPO2 mode. All of them are used to add redundancy and increase reliability in the HR mode. In order to reduce current consumption, the LEDs are sampled with a very low duty cycle and synchronized with the S&H. The ALR circuit is implemented in such a way that there is no need for a specific phase of ambient light acquisition and removal. Furthermore, the chosen topology relaxes flicker noise constraints that might be significant in MOS technology. The signal is recovered at the end of the chain with a simple LPF and digitized with an adequate ADC.

From this scheme, two points are key for the ASIC:

- The noise of the LED drivers and the TIA;
- The implementation of the LPF at the end of the chain.

During the LED switching-on phase, the photodiode current is the sum of the pulse rate signal (LED passing through the skin vessels), the ambient light (coming through the tissues directly to the photodiode), and the direct LED light (to the photodiode without passing through the skin vessels). Artifacts created by movements can saturate the chain and swamp the useful signal. To guarantee the needed dynamic, noise is a critical point, especially in front of the gain that is on the LED drivers and the TIA. A good trade-off between silicon area (see Figure 2) and current consumption has to be found to well balance flicker and thermal noise within the useful bandwidth.

The second critical point is the very low cutoff frequency required for the LPF. This implies a high RC time constant and, in turn, a huge silicon area. Resistance values are realized by switched capacitors, but increasing their values too much also increases thermal noise. Again, a trade-off should be made between noise, area and the need for external components. In this implementation, two external capacitors are needed, one after the S&H and one at the very end of the chain intended to prevent aliasing in the ADC.

The circuit has been integrated in TSMC 0.18 µm, standard CMOS process. Two supply voltages are needed, 3 V for the input TIA and the LED driver, 1.8 V for the rest of the system.

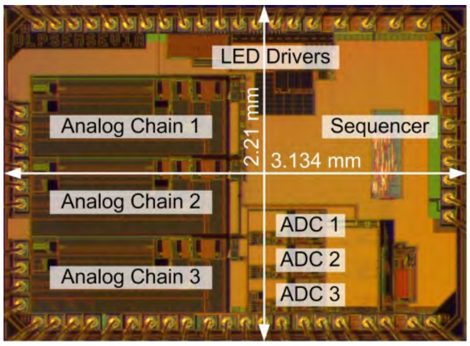

Figure 2: Die photography of the ASIC and area information (7 mm^2).

The measured analogue front end shows a consumption of 235 µA for the three analog chains and an output integrated noise lower than 10 µV$_{RMS}$ within the 5 Hz signal bandwidT. The three ADCs consume 530 µA for an input referred noise of 18 µV$_{RMS}$ within a 250 Hz bandwidth and a resolution of 15 bits. The ADC results are ready after 4 ms from the switching-on which allows duty cycling also on the ADCs. LED drivers can bias the IR and Red LED from a 200 µA PTAT current reference to respectively 20 mA and 120 mA in less than 30 µs, with noise level comparable to that of the TIA (good balance of noise along the chain).

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[1] R. Gentsch, P. Theurillat, "Pulsewatch IC preliminary specifications", internal report, (2011)