

22nm, <10nW, Switched Capacitance or Resistance-based Always-on Circuits for IoT

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The rapid growth of IoT devices mandates ultra-low-power (ULP) circuits to extend battery life and improve energy efficiency. Such edge nodes are further heavily duty-cycled to lower the average current and thus remain idle most of the time. This project focuses on the design of the few blocks that remains always-on and whose consumption should be further optimized with a sub-10 nW target in 22 nm CMOS, focusing on area-efficient techniques.

The expansion of IoT devices and applications is transforming modern technology, placing new demands on integrated circuit (IC) design. These devices typically operate on limited power sources such as small batteries or energy harvested from the environment. To achieve extended operational lifetime without frequent battery replacements, minimizing energy consumption is essential. Reducing power usage directly enhances battery longevity, which is important for the practicality and scalability of IoT technologies. A primary challenge in designing these devices is the integration of always-on components. These modules must remain active continuously, even when the device enters low-power sleep states, to perform essential functions like timekeeping, environmental sensing, and system wake-up operations. Reliable operation of these always-on blocks requires precise voltage and current references.

Designing such references poses unique challenges. Well-established topologies for Proportional to Absolute Temperature (PTAT) current references and bandgap (BG) voltage references typically rely on large resistors to operate at nanoampere (nA) level currents. Global Foundry's 22 nm FDSOI CMOS (GF22) is a trendy node to implement modern wireless sensors System-on-Chip for IoT at the edge. For always-on blocks, it provides advantages such as reduced leakage currents, minimized parasitics, and a wide body bias range, but it comes with high manufacturing costs making area efficiency critical. Alternative design techniques have thus to be leveraged to implement compact and thus cost-effective high ohmic resistors needed for always-on blocks.

This project addresses these constraints by developing ultra-low power and area-efficient voltage and current references through the substitution of large resistors with switched-capacitor and duty-cycled resistor architectures as pictured in Figure 1. These alternative techniques leverage clock frequency and duty cycle dependencies to achieve the required impedance for generating nW-level references, significantly reducing silicon area usage. By optimizing clock frequency, duty cycle, silicon area, and power consumption trade-offs, the design maintains sub-10 nW power dissipation.

The PTAT current reference, designed using MOSFETs operating in the subthreshold region, achieves less than 4 nW of power consumption and occupies just 0.001 mm² of silicon area. Subthreshold operation allows MOSFETs to efficiently manage extremely low currents while maintaining a high transconductance-to-current ratio.

For the bandgap reference, Bipolar Junction Transistors (BJTs) are utilized to achieve a stable voltage output resilient to process variations and device mismatches. A supply voltage of 900 mV is selected to match the end-of-life voltages of common batteries such as alkaline, silver oxide, and zinc-air, ensuring precise operation throughout the battery lifespan. The reference voltage is set to 800 mV to align with the supply requirements of RF Field-Effect Transistors (FETs) in GF22 and the system core voltage. The reference operates with a nominal power consumption of less than 8 nW, including the ring oscillator, and occupies 0.021 mm² of silicon area with over 2 G Ω of equivalent resistors. It achieves a temperature coefficient (TC) of 60 ppm/ $^{\circ}$ C and a line sensitivity of 0.56%/V. ULP is thus not incompatible with good performances.

Additionally, the bandgap reference serves as a stable voltage reference for a low-dropout (LDO) regulator. The LDO is designed to maintain low noise and high precision, ensuring that its output voltage remains stable despite variations in the supply voltage (ranging from 900 mV to 1.98 V) and low load currents (from 100 nA to 1 μ A). By utilizing unity-gain feedback, the LDO eliminates noise multiplication, enhancing the regulator's performance.

In conclusion, this project demonstrates that it is possible to achieve highly efficient, area-conscious sub-10 nW designs for always-on blocks in advanced semiconductor nodes. By carefully sizing the transistors to control leakage currents, utilizing the wide body bias range in FDSOI technology and focusing on innovative design approaches to replace traditional resistor-based techniques, this work lays the foundation for future development of energy-efficient circuits capable of supporting the next generation of IoT devices.

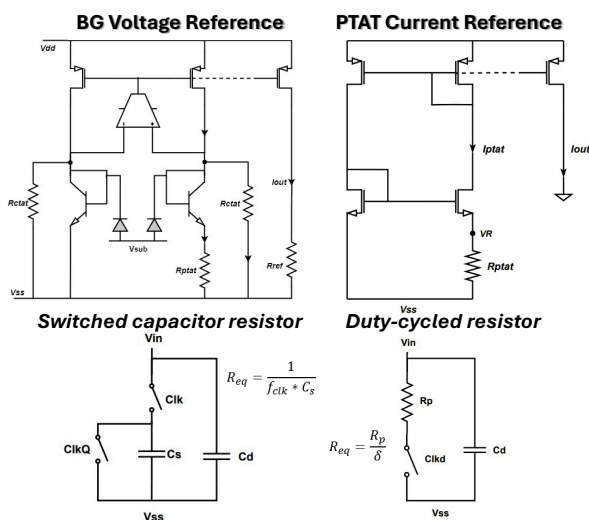


Figure 1: Schematic of the voltage and current reference and details about the switched capacitor or duty cycled resistor to implement compact over 500 M Ω equivalent resistances.