

A 24-GHz 4-Element Multi-Beam Wireless Energy Harvesting Array with Class-F Rectifiers Achieving 51.5% PCE

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Abstract—This paper presents a 4-element concurrent multi-beam energy harvesting array. The proposed architecture introduces three-line-couplers as the matching network to develop class-F waveforms and achieve 51.5% rectifier efficiency. A 4-port butler matrix with transformer-based 90° hybrid couplers is utilized to perform concurrent coherent beamforming. Implemented in a 22nm CMOS FD-SOI process, the proposed array can cover full FoV with 28dB peak-to-null ratio.

Keywords—WPT, Rectifiers, Energy harvesting, Butler matrix, PCE.

I. INTRODUCTION

The rapid growth of IoT devices over the past decade necessitates new ways to power these miniaturized devices. The massive environmental impact and maintenance cost of traditional batteries make them infeasible in practice for these trillion-scaled IoT devices. Far-field wireless power transfer (WPT) offers a viable alternative solution, as wireless power can be delivered by local gateway or even robots or drones in the future. While most reported WPT systems focus on RF solutions such as 2.4GHz [1], [2], [3], the limited area constraints on the IoT node leads to low efficiency for the receiving antennas. Mm-Wave WPT systems use smaller antennas and thus a higher gain and beamforming on the transmitter side, which in turn reduces the losses associated with the transmission and reception by focusing the total radiated power toward the receiver. Keeping a constant total receiving antenna array aperture size, the path loss due to the frequency increment will be totally compensated. However, moving toward high frequencies, both TX PA and RX rectifier start to degrade due to the device parasitics, which require judicious design innovations.

The synchronous half-wave rectifiers backscatter a considerable power level at even harmonics to the antenna, and they also exhibit additional loss and area overhead for 180° phase shifters [4]. Omitting these phase shifters results in higher loss (transistor saturation in conduction mode) and negative DC output. While the differential cross-coupled rectifier (CCR) removes 180° phase shifters, its performance is still limited to the device leakage during state transition, when the transistor is still conducting, and the drain voltage falls below output DC (Fig. 1a) [5]. This sets the fundamental limit of their PCEs to around 40% [5]. Reference [6] introduces

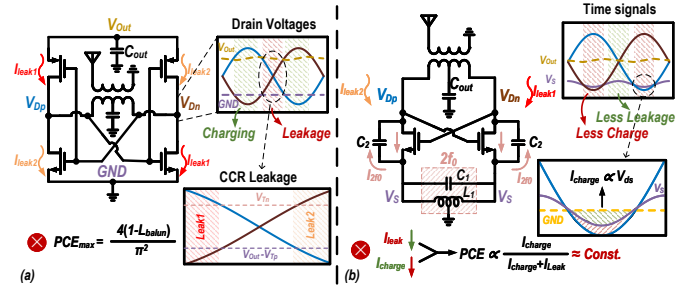


Fig. 1. The limitations of reported cross-coupled rectifier structures: a) NMOS/PMOS CCR [5]. b) 2nd Harmonic NMOS CCR [6].

a second harmonic resonance on the transistor's source to suppress leakage. However, it decreases both charging and leakage currents and results in a limited overall PCE improvement (Fig. 1b).

In this work, a 24GHz 4-element wireless energy harvesting array system using class-F rectifiers is proposed to leverage constructive passive beamforming networks to boost the total RX power conversion efficiency (PCE) and dynamic range with concurrent multi-beam harvesting capability, while simultaneously achieving the best reported PCE for each element.

II. CLASS-F RECTIFIER

Conceptually, square waveform on the drain node of CCR is desired as it leads to zero leakage while maximizing the charging current. Thus, this work targets the 3rd harmonic termination on the drain node to approach this desired waveform (180° 3rd harmonic on drain). However, this square signal is not suitable for gate driving as it limits the overdrive and increases the conduction loss. Shown in Fig. 2a, the leakage current of a conventional CCR has a notch at the AC zero crossing point due to limited overdrive. A lower drain/gate signal swing (V_{PP}) further limits this overdrive and the notch minimum falls to zero. This is why having a delay on the gate driving signal around the zero crossing, thanks to the 3rd harmonic voltage coupled with the drain node, further boosts the rectifier performance by expanding this notch for low V_{PP} . This concept is demonstrated by using the MOSFET quadratic model for simplicity. For low V_{PP} , the optimum

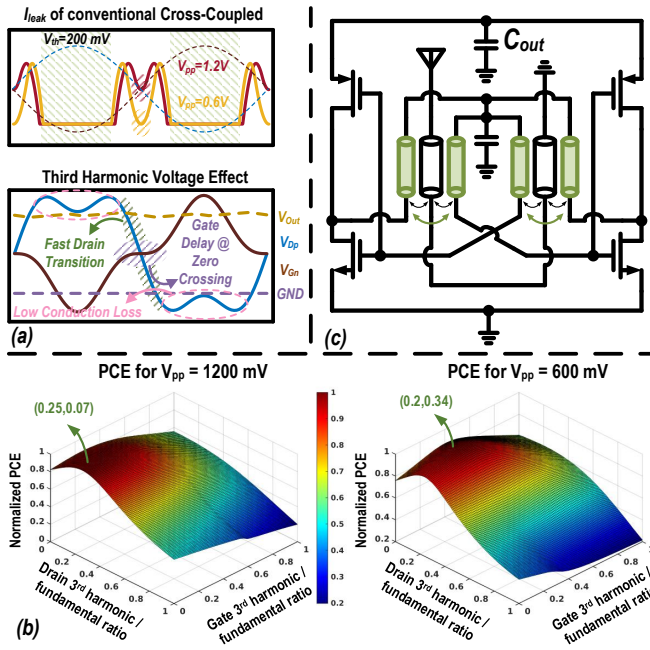


Fig. 2. Proposed class-F rectifier. a) 3^{rd} harmonic on S/D signals. b) Optimum PCE point. c) Three-coupled-line class-F rectifier schematic.

PCE point is where we have an in-phase 3^{rd} harmonic with respect to the fundamental signal on the gate (Fig. 2b). This paper introduces a Class-F CCR to implement these desired harmonic conditions and input matching integrated all together in just a compact three-coupled-line based input balun (Fig. 2c).

Compared to transformer-based baluns, coupled-line baluns consider both magnetic and electric effects and accurately model the wideband balun behavior, critical for achieving both fundamental driving at 24GHz and 3^{rd} harmonic termination at 72GHz. However, asymmetric

three-line-couplers entail high complexity and present limited design practices. For this application, we assume symmetry for the two side conductors (secondaries) around the center conductor (primary), which limits the design space to three fundamental mode impedances and a γ factor (Fig. 3a) [7]. Neglecting common-mode due to the antenna (which is acceptable based on CMRR simulation), the drain impedance could be simplified and derived. Two resonance points are formed on the drain impedance due to: 1) antenna-to-drain coupling 2) gate-to-drain coupling (Fig. 3b-c). In the B-Mode, since this impedance controls primary to secondary coupling and, its value controls first resonance peak. However, the C-Mode impedance controls gate-to-drain coupling (gate/drain residue inductance) and the second resonance frequency. By controlling these two impedances and the electrical length of the coupled line (which will move both resonance frequencies), one can independently control drain impedance and provide the optimum condition for operation without adding extra capacitance on either gate or drain (Fig. 3d). This is especially important since additional capacitances will increase drain/gate quality factor and results in higher matching loss.

III. CONCURRENT BEAMFORMING

Fig. 4 shows the system block diagram for the concurrent multi-beam energy harvesting array. With a small wavelength at 24GHz ($\lambda=1.25\text{cm}$ in air), increasing the antenna aperture leads to high-gain and highly directive antennas, which is undesired for WPT applications since it necessitates the flexibility for wireless power extraction from all directions. Another alternative is a rectenna array that directly connects each antenna to a rectifier and performs DC combining after rectification. While it increases the total antenna aperture size, hence the received power, it does not perform coherent beamforming and thus no array gain. Moreover, each rectifier only takes the received power within each element, resulting

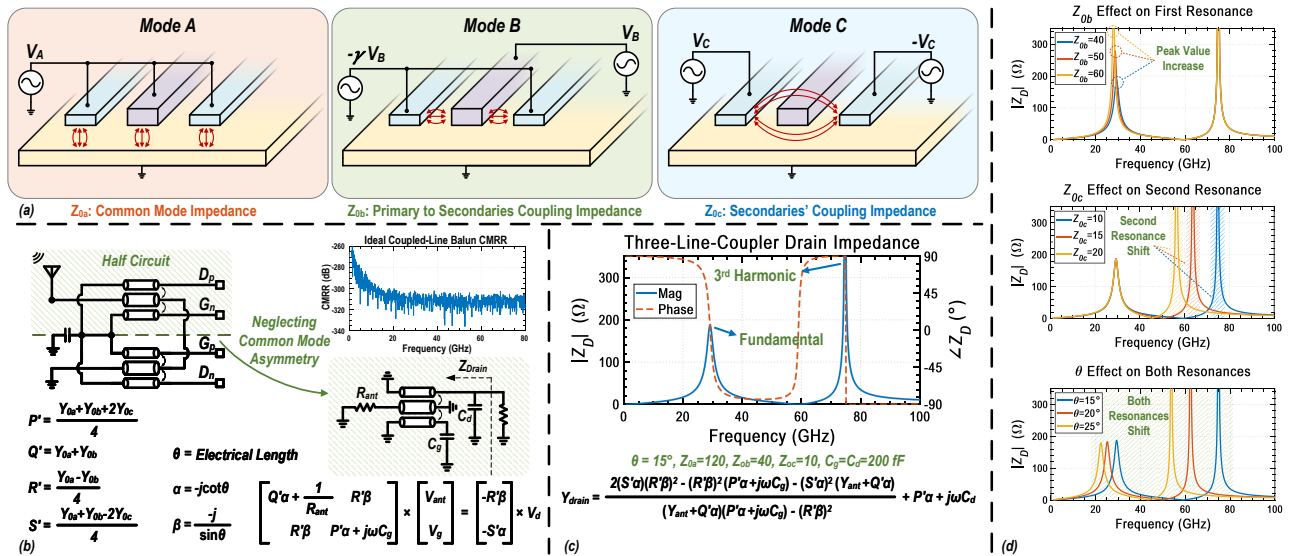


Fig. 3. Modeling of a three-line-coupler: a) Fundamental mode impedances. b) Z_{drain} equations. c) Z_{drain} two resonance point. d) Full control on Z_{drain} .

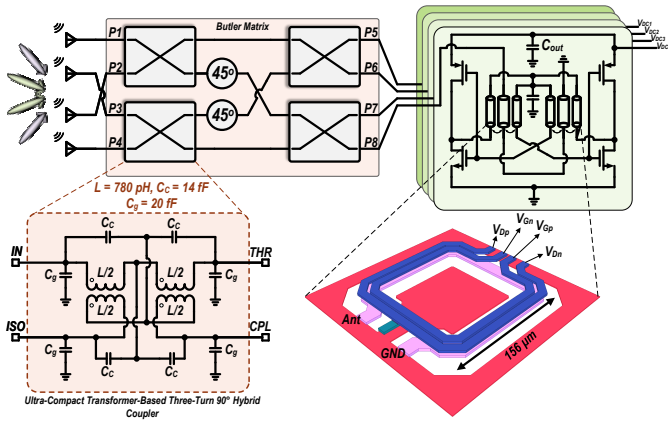


Fig. 4. Proposed concurrent multi-beam rectifying array.

in their limited PCE and sensitivity. Active array coherent beamforming, e.g., analog beamformers with phase shifters, achieves additional array gain yet at the expenses of high power consumption, which is also unsuitable for WPT applications.

In contrast, butler matrix as a coherent all-passive beamforming architecture, offers unique advantages for array-based WPT systems [8]. First, it offers zero-power and low complexity for its beamforming, ensuring low overhead and cold-start of the WPT RX array. Secondly, it concurrently forms multiple beams in different incident angles, meaning the WPT RX array can simultaneously receive wireless power from multiple sources and collectively cover the entire field-of-view (FoV). This is particularly beneficial in WPT RX arrays since incoming wireless power sources often come from unknown directions. Thirdly, placing the rectifiers after the passive beamformers will leverage the array gain and boost the received power signal, which in-turn increases the total PCE and sensitivity of the system. On the other hand, the loss of the passive beamformers needs to be minimized, requiring careful passive design and co-design with the rectifier circuits. The beamforming network is implemented using transformer-based 90° hybrid couplers as reported in [9].

IV. MEASUREMENT RESULTS

The 4-element concurrent passive beamforming rectifying array is implemented in a 22nm CMOS FD-SOI process with a core area/chip area of 0.53/0.85mm² (Fig. 5). Also, three separate test-structure are fabricated for single device and

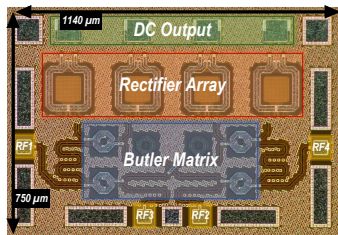


Fig. 5. Die micrograph of the proposed array.

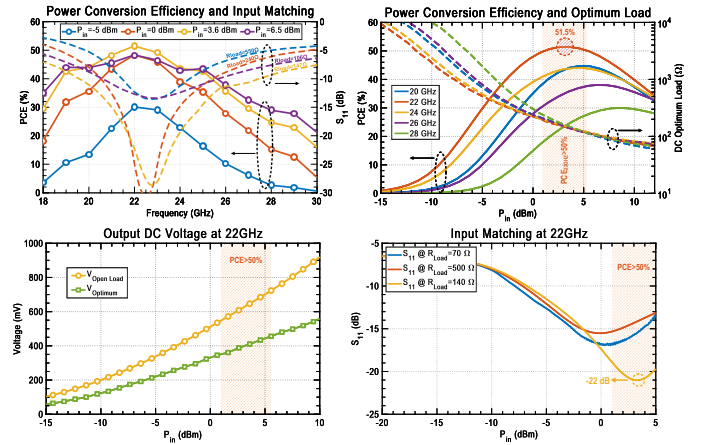


Fig. 6. Measured single rectifier performance across both frequency and input power variation.

beamforming network characterisation. All the measurements were performed using direct chip probing. The center frequency is shifted from 24GHz in simulation to 22GHz in measurement. Fig. 6 shows the measured performance for the single element rectifier. The measured PCE achieves 51.5% peak and optimum DC voltage of 410mV for an input power of $P_{in}=3.6\text{dBm}$ at 22GHz. The optimum DC load for this peak point is equal to 147Ω. The PCE curves are measured across both input power and frequency range. The rectifier achieves PCE 3dB BW of 17.5-28GHz at $P_{in}=3.6\text{dBm}$, while the input matching is better than -10dB over 19.5-27.5GHz. The optimum DC load varies from 80Ω to 10KΩ across shown input power range. The DC output voltages and input matching across input power range in shown for the 22GHz input signal. Considering 30% efficiency as a threshold for the dynamic range, the class-F rectifier achieves a dynamic range of -5dBm to 14dBm for 22GHz input signal.

The measured S-parameters for the butler matrix test

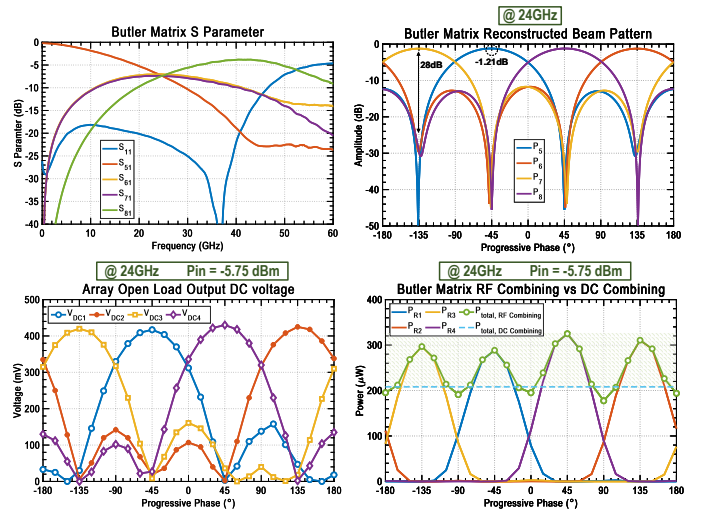


Fig. 7. Measured butler matrix s-parameter and reconstructed beam pattern based on measurements. Measured rectifying array performance across input progressive phases.

structures are shown in Fig. 7. Using two 4-way probing test-structures, the whole S-parameter of the butler matrix is reconstructed. The resulting beam pattern at 24GHz shows a passive loss of only 1.21dB for the beamformer with a peak-to-null ratio better than 28dB for all four main beams. The measurement results for the rectifying array are also shown in Fig. 7 for the power level of -5.75dBm at 24GHz on each of the input ports. The output DC open load voltages and the optimum output power for each of the rectifier elements are shown versus progressive phase of the input signals and the 4 beam peaks as depicted. The measurement results for the proposed array with coherent passive butler matrix beamforming shows rectified DC output power peaks as high as 310 μ W for the four main beam incidence angles, while keeping competitive performance even for in-between beam incidence angles.

A comparison of coherent beamforming array (proposed architecture) versus non-coherent rectifier array (rectenna array with DC combining) is also shown (Fig. 7). Assuming 4-element non-coherent rectifier, with Pin = -5.75dBm the output DC of each element is 52 μ W. Even with lossless DC power combining, the best total output power of the array is 208 μ W. It shows that the proposed design achieves an array improvement factor of 1.49 (310 μ W/208 μ W) for the beam peaks and an average of 1.18 (245 μ W/208 μ W) over all FoV.

V. CONCLUSION

Table 1 shows the performance comparison. Compared to the other mm-Wave rectifiers, this work achieves the highest PCE with the peak rectifier PCE of 51.5%. Moreover, while the reported rectifying arrays show limited efficiency with the best being 15%, the low-loss passive beamformer and its co-design in this work achieves high system PCE of 30.2% at Pin = -5.75dBm.

Table 1. Performance summary and comparison with the state-of-the-art mm-wave rectifier/rectifying arrays.

	This Work		IMS2022 [6]	JSSC2022 [10]	TMTT2019 [4]	IMS2023 [11]	TMTT2016 [5]
Technology	22nm CMOS FDSOI		65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS
Rectifier Topology	Class-F NMOS/PMOS Cross-Coupled		NMOS Coss-Coupled Harmonically-boosted	NMOS/PMOS Cross-Coupled	Synchronous	NMOS Cross-Coupled	NMOS/PMOS Cross-Coupled
Active Area (mm ²)	0.066 (Single)/0.53 (Array)		0.026 (Single)	N/A	0.074 (Single)	0.99 (Array)	N/A
Bandwidth (GHz)	10.5		13.5	N/A	11	N/A	N/A
Frequency (GHz)	22	24	28	24	35	24	60
PCE _{Max} (%)	51.5	44	40	15 ^c	36	12.2 ^d	32.8
P _{in} @ PCE _{Max} (dBm)	3.6	4	3	0	15	0	5.7
V _{DC, Optimum} (mV)	410	390	350	N/A	850	N/A	820
Dynamic Range ^b (dB)	19 (-5 to 14)	17 (-3 to 14)	14 ^{e,f}	N/A	6.5 ^{e,f}	N/A	N/A
Input Matching ^g (dB)	-22	-18	-17	N/A	-14 ^e	N/A	N/A
Array	Yes		No	Yes	No	Yes	No
Concurrent Beamforming	Yes		No	No	No	Yes	No
Array Number	4		1	4	1	4	1
Peak-to-Null Ratio (dB)	28		N/A	N/A	N/A	N/A	N/A
Beamforming Loss (dB)	1.21		N/A	1.8 ^e	N/A	N/A	N/A
Array Improvement Factor	1.49		N/A	N/A	N/A	N/A	N/A

a) 3dB Efficiency BW. b) Defined as PCE>30%. c) at peak PCE power
d) PCE Curve is measured up to 10dbm. e) Simulated. f) Measured in Array Mode
g) Small Signal Matching

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