

# 60-GHz FMCW Radar Platform Demonstrator for Presence Detection Applications

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This 60-GHz radar platform demonstrator is based on an ultra-low power RF front-end developed in GF 22-nm FDSOI CMOS technology. The system is completed with the baseband processing on FPGA and software to detect targets with a resolution of 1.9 cm up to several meters.

Radio detection and ranging (radar) systems operating in the millimeter wave (mmWave) frequency band have rapidly grown over the past years. Radars based on the frequency-modulated continuous-wave (FMCW) principle benefit from a multi-GHz bandwidth to achieve a range resolution in the order of a few millimeters. The 60-GHz industrial, scientific and medical (ISM) frequency band is one of the most used because of its large available spectrum, namely from 57 to 66 GHz, which corresponds to a nominal range resolution of 17 mm. This band is most suited for short-range devices, including applications such as vital signs monitoring, gesture recognition and smart-home applications [1].

Another important advantage of operating at mmWave is the miniaturization of integrated passive components and off-chip antennas. This aspect is crucial for the integration of several transmitter (Tx) and/or receiver (Rx) chains, allowing to recover the angle of arrival (AoA) and hence to localize the targets. In addition, harnessing the power of the multiple-input multiple-output (MIMO) processing, it is possible to achieve a high angular resolution with a limited number of Tx and Rx elements (denoted as N and M respectively). This is because the number of virtual antennas is equal to  $N \times M$ , which is very efficient area-wise for large arrays. The arrangement of the antennas can enable angular resolution in azimuth, elevation or both.

This radar platform is based on an ultra-low power 60-GHz 4Tx/4Rx MIMO radar system fabricated in GF 22-nm FDSOI CMOS technology. The integrated circuit (IC) is highly compact thanks to the modular design of Tx and Rx chains with an efficient distribution of the local oscillator, which facilitates the customization of the MIMO array. The total chip surface is  $2.5 \text{ mm} \times 1.25 \text{ mm}$ , while a Tx-Rx slice occupies  $0.4 \text{ mm} \times 1.25 \text{ mm}$ . The IC floorplan is designed to maximize the separation of Tx and Rx antennas while maintaining a small-sized PCB, which is crucial to mitigate the direct Tx-Rx coupling.

The key feature of this IC with respect to the other solutions available on the market is its ultra-low power consumption. While operating in the single-input single-output configuration (1Tx/1Rx), the system consumes 40.2 mW in continuous mode, while in the MIMO configuration (4Tx/4Rx), it consumes 101 mW. Thanks to the MIMO processing, the radar IC achieves a record low power consumption of 6.3 mW per virtual channel.

Figure 1 shows the top view of the demonstrator PCB. In the middle there is the IC, on which the whole RF front-end of the system is integrated, including the Tx and Rx chains and the frequency synthesis with FMCW chirp generator and crystal oscillator. Moreover, there are the patch antennas connected to the Tx and Rx I/O, spaced by  $3\lambda/2$  on the Tx side and by  $2\lambda$  on the Rx side. The distance between the virtual antennas is still

$\lambda/2$  to maximize the field of view, while the close-in sidebands are minimized. Most of the baseband (BB) chains, comprising the anti-aliasing band-pass filter with amplification and analog-digital converter (ADC), are designed on the PCB and placed on the back side. The ADC serial outputs are then connected to the I/O of a MicroZed board, which is based on the AMD Xilinx Zynq®-7000 system-on-chip and several peripherals.

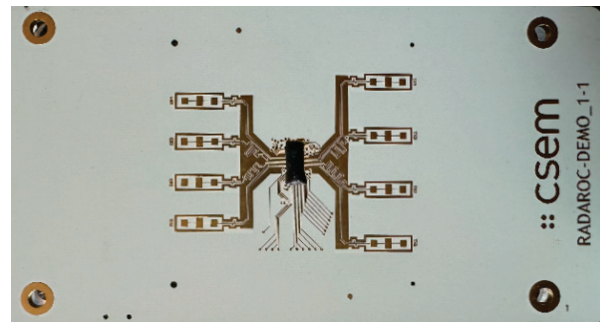


Figure 1: Radar demonstrator PCB.

The preliminary signal processing is carried out on the FPGA. After deserialization, the baseband signal is demodulated with the same codes used to modulate the chirp to separate the contributions coming from the respective Tx. Afterwards, the signals are filtered and decimated to greatly reduce the data rate. The rest of the radar processing is coded on a computer in real-time. Primarily, 3 FFT operations are needed to recover the so-called "radar data cube", i.e. the range-velocity-angle map. The first FFT on the BB signal allows to retrieve the range between the sensor and the targets. Then, a second FFT on the variation of the phase of the first FFT across consecutive chirps provides the radial velocity of the targets. Finally, once the range-Doppler map is available for each virtual antenna in the MIMO array, the third spatial FFT on the phase variations across the channels enables the extraction of the AoA. Figure 2 shows the demonstration of the radar range resolution: the system can distinguish 2 targets separated by 1.9 cm at 1m distance.

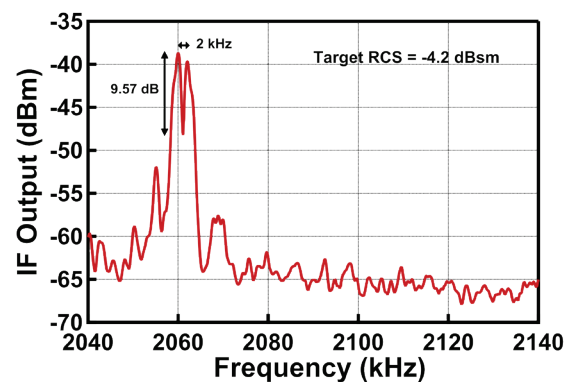


Figure 2: Radar platform range resolution.

[1] S. Cerida Rengifo, et al., An Ultralow Power Short-Range 60-GHz FMCW Radar in 22-nm FDSOI CMOS. IEEE TMTT 72-4 (2024) 2548